AMENDMENTS TO THE SPECIFICATION

Please amend the following paragraphs, in the specification, as follows:

Page 14, the paragraph beginning on line 11, please amend as follows:

A plurality of enable signals orderly delayed are created by serially connected ~~resistances R1 to R7 or~~ resistances R1 to R7 and R8 to R14 or several serially connected inverters.

Page 16, the paragraph beginning on line 17, please amend as follows:

As shown, in addition to the constitution elements described in Fig. 8, the semiconductor memory device in accordance with a forth preferred embodiment further includes a plurality of ~~first delay functions D1 to D3 and a plurality of second delay functions D4 to D6~~ first delay functions D1 to D3, e.g., R1 to R3, and D7 to D9, e.g., R7 to R9, and a plurality of second delay functions D4 to D6, e.g., R4 to R6, and D10 to D12, e.g., R10 to R12. The plurality of the first delay functions D1 to D3 are serially connected for turning on a plurality of switches 610a to 610d orderly at a first timing set by orderly delaying an output signal of the first sense amplifier control logic 530. The plurality of second delay functions D4 to D6 are serially connected for turning on a plurality of switches 610e to 610h orderly at a second timing set by orderly delaying a output signal of the second sense amplifier control logic 530'.

Page 17, the paragraph beginning on line 14, please amend as follows:

As shown, a second sense amplifier control logic 530' included in the semiconductor memory device is controlled by a signal ~~delayed by a signal controlling the first sense amplifier division 500~~ delayed by a delay equipment 540 which delays a signal outputted from a first sense amplifier control logic 530.